WEST Search History

| Hide Items | Restore | Clear | Cancel |

DATE: Tuesday, July 12, 2005

Hide?	Set Name	Query	Hit Count
		DB=JPAB; PLUR=YES; OP=ADJ	
⌐	L16	L15 and capaciti$	12
⌐	L15	L12 and (memory or cell)	278
⌐	L14	I10 and (memory or cell)	0
⌐	L13	L12 and (memory or cell)	278
⌐	L12	control gate and (sidewall$ or side wall$)	371
⌐	L11	L9control gate and (sidewall$ or side wall$)	0
		DB=USPT; PLUR=YES; OP=ADJ	
⌐	L10	L9 and (sidewall$ or side wall$)	43
⌐	L9	L8 and orthogonal	79
⌐	L8	L7 and floating gate	781
⌐	L7	L6 and direction$	822
⌐	L6	L5 and semiconductor	1289
⌐	L5	L4 and substrate	1358
⌐	L4	L3 and control gate	1657
⌐	L3	L2 and cell$	3122
⌐	L2	L1 and NAND$	3727
⌐	L1	memory and EEPROM	32545

END OF SEARCH HISTORY

WEST Search History

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DATE: Tuesday, July 12, 2005

Hide?	Set Name	Query	Hit Count
		DB=JPAB; PLUR=YES; OP=ADJ	
⌐	L18	L15 and opposite	16
⌐	L17	L15 and orthogonal	1
⌐	L16	L15 and capaciti$	12
⌐	L15	L12 and (memory or cell)	278
⌐	L14	I10 and (memory or cell)	0
⌐	L13	L12 and (memory or cell)	278
⌐	L12	control gate and (sidewall$ or side wall$)	371
⌐	L11	L9control gate and (sidewall$ or side wall$)	0
		DB=USPT; PLUR=YES; OP=ADJ	
⌐	L10	L9 and (sidewall$ or side wall$)	43
⌐	L9	L8 and orthogonal	79
⌐	L8	L7 and floating gate	781
⌐	L7	L6 and direction$	822
⌐	L6	L5 and semiconductor	1289
⌐	L5	L4 and substrate	1358
⌐	L4	L3 and control gate	1657
⌐	L3	L2 and cell$	3122
⌐	L2	L1 and NAND$	3727
⌐	L1	memory and EEPROM	32545

END OF SEARCH HISTORY